CLAIMS:

1. A method for providing clock signals to a mixed signal telecommunication chip having a communication signal in a communication signal band, said clock signals comprising a central clock frequency signal and sub-frequency signals which are multiples or divisions of said central clock frequency signal, wherein the central clock frequency signal is selected such that the central clock frequency signal and the sub-frequency signals are located outside the telecommunication signal band.

2. The method according to claim 1, where the telecommunication signal band is between 2,402 GHz and 2,480 GHz.

3. The method according to claim 1, where the central clock frequency is a multiple of 2.

4. The method according to claim 1 or 2, where the central clock frequency is in between 70 MHz and 90 MHz, preferably 64 MHz, 76 MHz or 80 MHz.

5. The method according to any of the preceding claims, wherein the central clock frequency is 64 MHz, the precision is 8 bit and the over-sampling factor is 32.

6. The method according to any of the preceding claims, the chip comprising functional circuit blocks, wherein the central-clock-frequency is supplied to the functional blocks by an on-chip oscillator (12)

7. A mixed signal telecommunication chip comprising as functional blocks a RF front end unit (2), an analog to digital converter (4), a digital to analog converter (6), a modulator/demodulator (8), a RF synthesizer (10) and an oscillator (12) for processing a communication signal in a communication signal band, wherein the functional blocks are fed by clock signals comprising a central clock frequency signal and sub-frequency signals which are multiples or divisions of said central clock frequency signal, and wherein the central

clock frequency signal and the sub-frequency signals are located outside of the telecommunication signal band.

8. The chip according to claim 7, wherein the telecommunication signal band is between 2,402 GHz and 2,480 GHz.

9. The chip according to claim 7 or 8, wherein the central clock frequency is a multiple of 2.

10. The chip according to any of the claims 7 to 9, wherein the central clock frequency is in between 70 MHz and 90 MHz, preferably 64 MHz, 76 MHz or 80 MHz.

11. The chip according to any of the claims 7 to 10, wherein the central clock frequency is 64 MHz, the precision is 8 bit and the over-sampling factor is 32.

12. The chip according to any of the claims 7 to 11, wherein the D/A converter is directly connected to the RF front end portion.

13. The chip according to any of the claims 7 to 12, comprising an on-chip-oscillator supplying the central clock frequency to the functional blocks.

14. The chip according to any of the claims 7 to 13, wherein the on-chip oscillator is connected to an external oscillator.

15. The chip according to any of the claims 7 to 14, wherein the external oscillator is a crystall oscillator.